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JC997 U.S. PTO
09/884172

06/19/01

438	Class	Subclass	ISSUE CLASSIFICATION
285			

PM

PATENT NUMBER

6649480

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
202 O.A. TM	NOV 18 2003

APPLICATION NO. 09/884172	CONT/PRIOR D	CLASS 285	SUBCLASS 285	ART UNIT 2811	EXAMINER
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APPLICANTS
Eugene Fitzgerald
Nicole Perish

TITLE
Method of fabricating CMOS inverter and integrated circuits
utilizing strained silicon surface channel mosfets

PTO-2040
12/99

ISSUING CLASSIFICATION							
ORIGINAL				CROSS REFERENCE(S)			
CLASS		SUBCLASS		CLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)	
438		285		438		199	
INTERNATIONAL CLASSIFICATION							
H01L		21/356					
Continued on Issue Slip Inside File Jacket							

Formal Drawings (sheets) 13

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	13	21	13a-e	23	1
	NOTICE OF ALLOWANCE MAILED				
The term of this patent subsequent to (date) Christopher Lallin 6/13/03 (Assistant Examiner) has been disclaimed.			6-6-03		
The term of this patent shall not extend beyond the expiration date of U.S. Patent. No.			ISSUE FEE		
John F. N. Collins (Primary Examiner)			Amount Due	Date Paid	
1000			9-4-03		
The terminal months of this patent have been disclaimed.			ISSUE BATCH NUMBER		
Canton 6/03 (Legal Instruments Examiner)					

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